PATENT

Atty Docket No.: 10005208-1
App. Ser. No.: 09/891,325

IN THE CLAIMS:

Please find below a listing of all of the pending claims. The statuses of the claims are set forth in parentheses.

1. (Currently Amended) An on-chip capacitor comprising:

a first electrode formed during a first deposition of a first metal layer of a multi-level semiconductor device;

a first dielectric layer deposited on an interface of said first electrode, the first dielectric layer having a first dielectric constant;

a second electrode formed during a second deposition of a second metal layer of said multi-level deposition device, wherein said second electrode is deposited on an interface of said first dielectric layer, wherein said on-chip capacitor is formed in a crossover area of said first metal layer and said second metal layer of said multi-level semiconductor device; and

a second dielectric layer also deposited on the interface of said first dielectric layer, ~~the second dielectric layer having a second dielectric constant smaller than the first dielectric constant of the first dielectric layer~~.

2. (Original) The on-chip capacitor according to claim 1, wherein an angle of intersection between said first metal layer and said second metal layer is between zero and ninety degrees.

3. (Original) The on-chip capacitor according to claim 1, wherein said first electrode and said second electrode are configured to be substantially parallel.

4. (Original) The on-chip capacitor according to claim 3, wherein said first electrode and said second electrode are further configured to be overlapping.

5. (Original) The on-chip capacitor according to claim 1, wherein said first electrode and said second electrode are configured as a rectangular planar structure.

6. (Original) The on-chip capacitor according to claim 5, wherein said first electrode and said second electrode are substantially parallel and overlapping.

7. (Previously Presented) The on-chip capacitor according to claim 1, wherein said first dielectric layer comprises a composite of materials.

8. (Previously Presented) An on-chip capacitor comprising:

a first electrode formed during a first deposition of a first metal layer of a multi-level semiconductor device;

a substantially thin dielectric layer configured to be deposited over said first electrode; and

a second electrode formed during a second deposition of a second metal layer of said multi-level deposition device, wherein said second electrode is formed over said substantially thin dielectric layer, wherein said on-chip capacitor is formed in a crossover area of said first metal layer and said second metal layer of said multi-level semiconductor device; wherein said substantially thin dielectric layer comprises a composite of materials that includes PZT and platinum.

9. (Previously Presented) The on-chip bypass capacitor according to claim 1, wherein a dielectric constant of said first dielectric material layer is substantially high.

10. (Previously Presented) The on-chip bypass capacitor according to claim 9, wherein said first dielectric material layer includes silicon nitride.

11. (Previously Presented) The on-chip bypass capacitor according to claim 10, wherein said thickness of said first dielectric material layer is between 50 to 100 angstroms.

12. (Previously Presented) The on-chip capacitor according to claim 1, wherein the second electrode is also deposited on an interface of the second dielectric layer, and the second dielectric layer is predetermined to be thicker than the first dielectric layer.

13. (New) The on-chip capacitor of claim 1, wherein the second dielectric layer has a second dielectric constant that is smaller than the first dielectric constant of the first dielectric layer.